BCA [SEC]

[NEP-CBCS]

B.Sc. First Semester End Examination-2023

PAPER: BCA-SEC1T

[Digital Electronics]

Full Marks: 40 ***Time: 02 Hrs***

The figures in the right hand margin indicate marks

Candidates are required to give their answers in their own words as far as practicable

Illustrate the answers wherever necessary

Group A

1. Answer any FIVE questions of the following: **5x2= 10**

i) For an *n*-inputs X-NOR gate, $N \geq 2$, when will the out put be high?

ii) A = 01100010, B = 01011110. Find $\overline{A-B}$.

iii) Consider an 8 bit register R, that contains Excess – 128 code of – 12 . Show the content of R register.

iv) How does a sequential circuit differ from combinational circuit?

v) Find binary equivalent of $(206.25)_{10}$. Find decimal equivalent of $(101001.101)_2$.

vi) what is the need of clock signal in a sequential circuit?

vii) Define: (r-1's complement of a number, Where r is the base of the number system

viii) What is meant by overflow? Give an example to illustrate it.

Group B

Answer any FOUR questions of the following: **4x5 = 20**

2) Show the truth table of a full subtractor. Design a full subtractor using two half subtractors.

3) Is the expression $F_1 = w \cdot x + x \cdot \overline{y} \cdot \overline{z}$ is in sum of product (SOP) from? Justify your answer. Simplify the Boolean function $F(a,b,c,d) = \sum(m_1, m_2, m_5, m_7, m_{10}, m_{11}, m_{12})$ using Karnaugh map. 1+1+3

4) What is the role of an nx1 multiplexor circuit? It is required to implement $F(x,y,z) = \begin{cases} x, if\ z = 0 \\ y, if\ z = 1 \end{cases}$

Can multiplexor be used for this task? If yes, then show your circuit. 1+4

5) In IEEE-754 single precison representation, total 32 bits are used, out of which 23 bits are used for mantissa and 8 bits are used for Exponent. Show the representation of decimal floating point number – 36.25 using IEEE-754 32 bit representation.

6) Design a circuit that converts 3-bit binary code into equivalent gray code.

7) Sketch the logic system of a clocked SR flip-flop. Also write down the characteristics equation of SR flip-flop. What advantage does a JK flip-flop have over an SR flip-flop? How do SR, JK and D flip-flops differ? 2+1+1+1

Group C

Answer any ONE question of the following: **1x10 = 10**

8) a) Design a 4-bit CLA. Compare and contrast between serial and parallel adder. 5

b) Design a 4-bit left shift register. Show timing diagram. 3+2

9) a) Design a modulo – 10 counter.

b) Write a short note on IC design and fabrication process. 5+5
