2024

BCA

BCA First Semester End Examination - 2024

PAPER - CC102T

Computer Architecture

Full Marks : 40 *Time : 2 hours*

The figures in the right-hand margin indicate marks.
Candidates are required to give their answers in their own words as far as practicable.
Illustrate the answers wherever necessary.

Group-A

Attempt any five questions : 5×2=10

1. a) What is temporal locality?

   b) Suppose A=10111001, B=11010111. Find $\overline{A-B}$.

   c) A=01100010, B=01011110. Find $\overline{A} \oplus \overline{B}$.

   d) Consider an 8-bit register R, that contains Excess-128 code of –12. Show the content of R register.

   e) How does a sequential circuit differ from combinational circuit?

f) Find binary equivalent $(120.25)_{10}$. Find the decimal equivalement of $(1001.111)_2$.

g) What do you mean by write through cache?

h) What is the role of PC register?

Group-B

Attempt any four questions. **4×5=20**

2. Show the truth table of a full adder. Design a full adder using two half adders. 2+3

3. How does von Neumann architecture differ from Harvard architecture? What do you understand by instruction execution cycle? 3+2

4. What is the rule of SP register? It is required to implement

$$F(x,y,z) = \begin{cases} x, & \text{if } z = 1, \\ y, & \text{if } z = 0 \end{cases}$$

Use appropriate multiplexer for this task and show your circuit. 1+1

5. Draw and explain the memory hierarchy and explain its need. 2+2+1

6. What do you mean by cache miss? Suppose a cache memory has 75% hit rate, hit time=25 mili seconds and miss penalty time =45 seconds. Determine effective cache memory acces time. 2+3

7. Design a circuit converts 3-bit binary code into equivalent gray code.

Group-C

Attempt any one question. **1×10=10**

8. a) Realize the expression $(a+\bar{b}).\bar{c}$ using only NOR gates. 5

   b) Implement the Boolean function $F(a,b,c,d)=\Sigma(m_2,m_4,m_6, m_8,m_{10},m_{12},m_{14})$ using an 8×1 multiplexer. 5

9. a) Suppose, a CPU has word size 8-bit and is connected with a memory of size 4 KB. What will be the minimum length of memory data register and memory address register for this system? What do you understand by big endian memory organization? 2+2+2

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b) A CPU employs 5-stage instruction pipeline execution where time taken by opcode fetch, instruction decode, read operand, execute operation and write result stages are 4 ms, 2 ms, 3ms, 2 ms, 5 ms respectively. A program P consists of 600 instructions all of which are non-branching instructions. Calculate the total execution time of P. 4

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